FACULTY PROFILE

Name of the faculty: Dr. M. DAMODHAR RAO

Department: Electronics and Communication Engineering.
College: Gudlavalleru Engineering College
Phone No: 08674-273737/273888.
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Address for Communication

M.DAMODHAR RAO,
BUDDALAPALEM,
MUNJULURU POST,
MACHILIPATNAM,
KRISHNA- 521369. A.P.

Academic Qualifications

S. No	Name of the Degree *(Starting from Ph.D to 10th Class)*	College/ University	Percentage of Marks/Grade	Specialization	Year of Pass
1	Ph. D	JNTUK Kakinada	--	Low Power VLSI Design	2025
2	M. Tech	SRGEC Gudlavalleru	69.02%	Embedded Systems	2012
3	B.Tech	QISCET Ongole	66.07%	ECE	2008
4	Diploma	AANM & VVRSR Polytechnic Gudlavalleru	71.55%	DECE	2005
5	SSC	Board of Secondary Education	68.55%	--	2002

Professional Experience

S. No	Designation	Institution Name	Working Period	
			From	To
1	Associate Professor	SR Gudlavalleru Engineering College	01-05-2025	Till date
2	Assistant Professor	SR Gudlavalleru Engineering College	18-10-2012	30-04-2025
3	Assistant Professor	BIET, Bhimavaram	14-10-2011	15-10-2012

Academic Rewards / Achievements:

- ✓ Qualified GATE – 2009 in Electronics & Communication Engineering (EC).
- ✓ Achieved top 5% for the subject CMOS Digital VLSI Design with 75% (Elite + silver).

Professional Body Membership

S. No	Name of the Professional body	Membership Number
1	**Associate member of IEI**	**AM 162846-4**

Academic Identity:

- SCOPUS ID: **57216365892** https://www.scopus.com/freelookup/form/author.uri?zone=TopNavBar&origin=NO%20ORIGIN%20DEFINED
- ORCID Id: 0000-0003-2466-2562 (https://orcid.org/my-orcid?orcid=0000-0003-2466-2562)
- VIDWAN-ID : 198175 (https://vidwan.inflibnet.ac.in//profile/198175/MTk4MTc1)
- Web of Science Researcher ID: GLT-7993-2022 https://www.webofscience.com/wos/author/record/GLT-7993-2022
- Research Gate: https://www.researchgate.net/profile/Damu-Manda
- Google Scholar: https://scholar.google.com/citations?user=7YeTcH0AAAAJ&hl=en

Papers Published in Journals No.: 13 (SCI-1, Scopus-4)

1. **M.Damodhar Rao**, Y.V. Narayana, V.V.K.D.V. Prasad, "Ultra Low Power offering 14nm Bulk Double Gate FINFET based SRAM cells", Sustainable Computing: Informatics and Systems. Volume 35, September 2022, 100685.DOI: 10.1016/j.suscom.2022.100685 **(SCI)**

2. **M.Damodhar Rao**, Y.V. Narayana, V.V.K.D.V. Prasad, "Novel low power data retention regulating mechanism using DR-VDR in SRAM design" Journal of Advanced Research in Dynamical and Control Systems, Volume 12, Issue 2, pp: 823-834, 2020. DOI:10.5373/JARDCS/V12I2/S20201102 **(SCOPUS)**
3. **M.Damodhar Rao**, Y.V. Narayana, V.V.K.D.V. Prasad, "FinFET based SRAM cells design in various topologies using different power reduction techniques" Journal of Autonomous Intelligence (2024) Volume 7 Issue 1. DOI: 10.32629/jai.v7i1.976. **(SCOPUS)**
4. **M.Damodhar Rao**, Y.V. Narayana, V.V.K.D.V. Prasad, "Impact of Supply Voltage on SRAM Cell Power Dissipation Under Different Topologies" Telecommunications and Radio Engineering 83(5):57–69 (2024). DOI: 10.1615/TelecomRadEng.2024049360. **(SCOPUS)**
5. N, Indu, **Damodhar Rao M**, and Prasad V. V. K. D. V "High Speed Power Efficient Dynamic Comparator With Low Power Dissipation and Low Offset". Metallurgical and Materials Engineering 31 (3):112-18. 2025. https://doi.org/10.63278/1332. **(SCOPUS)**
6. **M. Damodhar Rao**, Ramireddi Vinod, Sk. Yasir, Y. Sai Sandeep and Sk. Haider Ali Saheb "Design And Performance Analysis of Power Gating Based 6T And 8T SRAM Cell" Industrial Engineering Journal, Volume 54, Issue 4, No. 1, April 2025. ISSN: 0970-2555. (**UGC Care**)
7. **M. Damodhar Rao**, Ch. Bhavana, A.Srilakshmi, B. Pravalika, A. Ravindranadh Tagore " Automatic Medicine Reminder and Recommender in critical health conditions" International Journal of Applied Science Engineering and Management, Vol 18, Issue 2, April 2024. ISSN: 2454-9940. (**UGC Care**)
8. **M. Damodhar Rao**, K. Keerthi Srujana, G. Navya Sree, N. Navya Sri, K. Nikhil Sai "Smart Electronic Noticing System Through Voice Alert and Text Message" International Journal of Research in Applied Science & Engineering Technology, Volume 12, Issue IV, April 2024. ISSN: 2321-9653. (**UGC Care**)
9. **M. Damodhar Rao**, Dr. V.V.K.D.V. Prasad, M. sudheer Kumar Reddy, N. Yogitha, N.Venkata Gurga Karthik, P. Dhanunjay " Low Power 7T SRAM Cell Design" Industrial Engineering Journal, Volume 52, Issue 4, No. 4, April 2023. ISSN: 0970-2555. (**UGC Care**)
10. Beram Eswar Charan Teja, **M. Damodhar Rao**, Dr. Y. V. Narayana, Dr. V. V. K. D. V. Prasad " Design and Implementation of Improved SRAM Cell "International Journal of Engineering Science and Computing, ISSN 2321 3361 © 2017 IJESC, volume 7, Issue no 6, June 2017 (**UGC Care**)
11. M.Vinay Babu, **M.Damodhar Rao**, Dr.V. V. K. D. V. Prasad "A Novel Architecture of 16-Bit Multiplier Using Modified Gate Diffusion Input Logic "IRACST-International Journal of Computer Science and Information Technology & Security(IJCSITS),ISSN : 2249-9555, Vol.6, No.4, July-August 2016, Pages: 69 - 74.
12. **M.Damodhar Rao** and R.Vijay " A Low Power 32-Bit Ripple Carry Adder Using Dynamic DML CMOS Logic Gates", International journal of Research-IJR, p-ISSN:2348-6848, e-ISSN: 2348-795x, vol-03,Issue 10, June 2016.
13. **M.Damodhar Rao** and G.Manasa "Design and analysis of fast addition mechanism for integers using quaternary signed digit number system", International journal of VLSI and Embedded systems-IJVES, vol-05, Article 09455, October 2014.

Papers Published in Conferences No.: 01

1. **M. Damodhar Rao** and V.Vittal Reddy, "Implementation of Improved Redundant binary Booth Encoding For Fast Multiplier", International Conference on Emerging Trends in Electronics, Communication and Computing Technology (ICECCT-11) on September 12-13 2011.

Patents Published No.: 02

1. M. Damodhar Rao, Dr. Y.V. Narayana, Dr. V.V.K.D.V. Prasad published a patent titled "Low Power SRAM Cell design for Embedded System Applications" on 15-07-2022.
2. Seshadri Rao Gudlavalleru Engineering College, Dr. K. Naga Prakash, Dr. Ch. Balaswamy, K. Rushendra Babu, M. Damodhar Rao, B. Nagasirisha published a patent titled " Band width Expansion System for Communication Medium and Method Thereof" on 16-09-2022.

Workshops /Conferences /Seminars Attended No.: 15

1. Five day Faculty Development Program (FDP) on "Optimized Solutions for IC Design with hands-on session on CMOS Design" organized by E&ICT Academy, NIT Warangal, Telangana in association with JNTUK, Kakinada, Sponsored by Ministry of Electronics and Information Technology (MeitY) GoI during 3rd to 7th February 2025.
2. Five days faculty Development Programme (FDP) on "Emerging Technologies in Electronics Engineering", organized by Godavari Institute of Engineering & Technology (A) from 29-06-2021 to 02-07-2021.
3. One week faculty Development Programme (FDP) on "Advanced CMOS VLSI" organized by E & ICT Academy, NIT Warangal at, NIT Warangal during 3rd -8th December 2018.
4. One week faculty Development Programme (FDP) on "Communication and signal processing" organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 29th October to 3rd November 2018.
5. Five days faculty Development Programme (FDP) on " CMOS Integrated circuits for Instrumentation and IoT applications" organized by E & ICT Academy, NIT Warangal at, velagapudhi Ramakrishna Siddhartha Engineering College, vijayawada during 22 nd – 28 th January 2018
6. Two week Online workshop on " CMOS,Mixed signal and radio frequency VLSI Design" organized by IIT Kharagpur, during 26th December 2016 to 4th February 2017.
7. Two day staff training program on " Simulation of Linear & Digital Integrated Circuits and Microcontroller based Applications" using NI Multisim " organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru on 4-5 November 2016.
8. Five days faculty Development Programme (FDP) on " Development of Wireless Sensor Networks using Network Simulator(NS2)- Hands On Experience" organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 1st–5th December 2015.

9. One Week Refresher course on "Microprocessor & Microcontrollers" organized by department of ECE, Gudlavalleru Engineering College, Gudlavalleru during 17th-21st November 2015.
10. I have attended a workshop on "Ultra Low Power Communication using CC430 Microcontroller: Hands on Experiences" organized by the ECE Dept. of Gudlavalleru Engineering College, held on 7th February 2015.
11. I have attended a workshop on "Speech Processing: Current Challenges and Hands on Experiences" organized by the ECE Dept. of Gudlavalleru Engineering College, held on 23rd August 2014.
12. I have attended a three-day national level workshop on "Theory & applications of Intelligent Signal Processing" organized by the ECE Dept. of Gudlavalleru Engg. College, Gudlavalleru held during 28th February - 02ndmarch December 2014.
13. Attended two-week Refresher course on "Electronics Devices and Circuits" during 23rd - 28th September, 2013 at Gudlavalleru Engineering College.
14. Attended a Two Day workshop on "Issues in Integrated Circuits (Ics) Design" during 13th – 14th December, 2013 at Gudlavalleru Engineering College.
15. Attended a workshop on "Signals & Systems" during 2nd -12th January, 2014 conducted by Indian Institute of Technology Kharagpur at Gudlavalleru Engineering College.

Certifications/Training Programs Attended No.: 05

1. **Attended Three Months Faculty Industrial training program on KEIL & ARM Processor from 27-01-2023 to 27-04-2023 at Efftronics Systems Pvt. Ltd.**
2. Certified in Five subjects through NPTEL program and got top 5% grade in CMOS digital VLSI design subject with Elite + silver Grade.
3. Training program on "Evaluating students' performance and designing question papers", Organized by National Institute of Technical Teachers Training and Research, Kolkata during 25th February to 1st March 2019.
4. Training program on "Development of wireless sensor networks simulator (NS2)"- Hands on experience, organized by Gudlavalleru Engineering College, Gudlavalleru during 01st – 05th December 2015.
5. Training program on "Training Teachers for Excellence", organized by Gudlavalleru Engineering College, Gudlavalleru during 17th- 21st June 2013.

Online FD/Webinar/Training programs No.: 08

1. One day Webinar on " Successful steps towards high quality scientific publications" by Dr.B.T.P.Madhav, Professor and Associate Dean, Academic Research, K L Deemed to be University, organized by Chalapathi Institute of Technology, Mothadaka, Guntur on 18th May 2020.
2. A Three day FDP on " VLSI Digital Circuits and Testing Techniques" organized by Miracle Education Society Group of Institutions, held from 21st to 23rd may 2020.

3. One week faculty Development Program (FDP) on “Recent trends in VLSI and Embedded Auto Industry” organized by organized by the Centre for VLSI and Embedded Systems Design (CVESD) in association with Dept. of ECE, CMR Technical Campus, Hyderabad from 20th to 24th of May, 2020
4. Participated a webinar on “Radio Frequency Measurements for Cellular and Wireless Communication Systems" organized by Department of Electronics and Communication Engineering on 25th May, 2020.
5. One week International online knowledge development program on “ Challenges and advancements in the design of IoT, Embedded and VLSI systems: A Researchers View” organized by Gudlavalleru Engineering College, Gudlavalleru during 08^{th} – 13^{th} June 2020.
6. One week National level online knowledge development program on “ Cyber Security” organized by Gudlavalleru Engineering College, Gudlavalleru with Cyberpsy, during 22^{nd} – 26^{th} July 2020.
7. One day Webinar on “ loe Power VLSI Circuits & Energy Harvesting for IoT Applications” organized by Department of Electronics and computer Engineering, sreenidhi institute of Science and Technology, Hyderabad eld on 15^{th} August 2020.
8. Participated in AICTE sponsored Online Short Term Training Programme on "Blockchain Architecture Design and Use Cases" Phase-I organized by Department of Electronics and Communication Engineering from 10-08-2020 to 15-08-2020.

Reviewer of Journals/ Conferences:

1) “Sustainable Computing: Informatics and Systems” An International Journal indexed in Science Citation Index Expanded, Scopus with 10.7 Cite Score and 3.8 Impact Factor ISSN: 2210-5379.

Subjects Handled

- Microprocessors and Microcontrollers.
- Radar Systems.
- Semiconductor devices and circuits.
- Computer Organization and architecture.
- Analog and Digital IC applications.
- Elements of Electronics Engineering.
- Pulse and Digital Circuits.
- Linear and Digital IC Applications.
- Embedded System Design.

Labs Handled

- Microprocessor and Microcontroller Lab.
- IC Applications Lab.

- Electronic Devices and Circuits Lab.
- EC&PDC Lab.
- VLSI design Lab.
- Digital Circuit Design Lab.

Other Responsibilities

College Level

1. UPS Coordinator.

Department Level

1. ISL-IoT LAB In-Charge.
2. Students Counselor.
3. IV Year Academic Coordinator.
4. Internship Coordinator.

Projects Guided

Under Graduation: 11

S. No	Name of the project	Year
1	Child Distance Monitoring And Alerting System	2014
2	Vehicle Accident prevention using IR sensor.	2015
3	Spying ROBOT with night vision wireless camera by android application	2016
4	Automatic Aquaculture managing system	2019
5	Lossless data compression and decompression	2019
6	Drudgery Reduction Vehicle for Rural Women	2020
7	Smart Gadget for Women Safety Using IoT	2020
8	Performance analysis of Low power SRAM cell at 45nm technology	2022
9	Low power SRAM design under different topologies	2023
10	Automatic Medicine Reminder and Recommender in critical health conditions	2024
11	Smart Electronic Noticing System Through Voice Alert and Text Message	2024

Post-Graduation: 2

S.No	Name of the project	Year
1	Design and analysis of fast addition mechanism for integers using quaternary signed digit number system	2015
2	A Novel Architecture of 16-Bit Multiplier Using Modified Gate Diffusion Input Logic	2016

Books Published No. : 03

1. Co-author for chapter 3.2 and 3.3 titled " Pulse And Digital Circuits Laboratory" of Electronics and Communication Engineering laboratory manual series 2 with ISBN-978-1-4276-5564-6 in the year 2016.
2. Co-author for chapter 21 titled " Radar Systems "of Electronics and Communication Engineering laboratory manual series 2 with ISBN-978-1-4276-5539-4 in the year 2016.
3. Co-author for chapter 2.1 titled "Electronic circuit and Pulse And Digital Circuits Laboratory" of Electronics and Communication Engineering laboratory manual series 2 with ISBN-978-1-4276-5536-3 in the year 2016.

Declaration

I hereby declare that all the above-furnished information is correct to the best of my knowledge.

Date : 03-06-2025. Signature

Place : Gudlavalleru. (Dr. M. Damodhar Rao)